Abstract

A highly parallel data processing system includes an array of n processing elements (PEs) and a controller sequence processor (SP) wherein at least one PE is combined with the controller SP to create a Dynamic Merged Processor (DP) which supports two modes of operation. In its first mode of operation, the DP acts as one of the PEs in the array and participates in the execution of single-instruction-multiple-data (SIMD) instructions. In the second mode of operation, the DP acts as the controlling element for the array of PEs and executes non-array instructions. To support these two modes of operation, the DP includes a plurality of execution units and two general-purpose register files. The execution units are "shared" in that they can execute instructions in either mode of operation. With very long instruction word (VLIW) capability, both modes of operation can be in effect on a cycle by cycle basis for every VLIW executed. This structure allows the controlling element in a highly parallel SIMD processor to be reused as one of the processing elements in the array to reduce the overall number of transistors and wires in the SIMD processor while maintaining its capabilities and performance.